Amendments to the Specification:

Please replace the paragraph beginning on page 2, line 16, with the following paragraph:

--Particularly high speeds can be achieved with so-called RISC processors. These processors have a reduced instruction set, and allow the use of hard-wired hardware to replace ~~microprogams~~ microprograms, in which the instructions to be processed are normally decoded and executed. This, in turn, allows the implementation of particularly fast and efficient instruction pipelines and instruction execution units, so that it is possible to execute an average of up to one instruction per processor cycle. However, even with RISC processors, it is not possible to execute more than one instruction per processor cycle due to the sequential nature of both processing and results that continues to apply.--